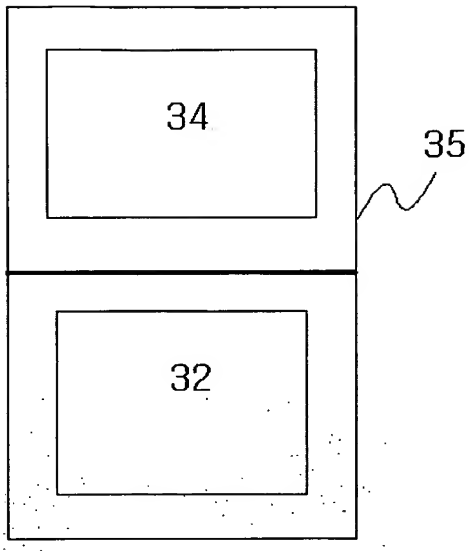
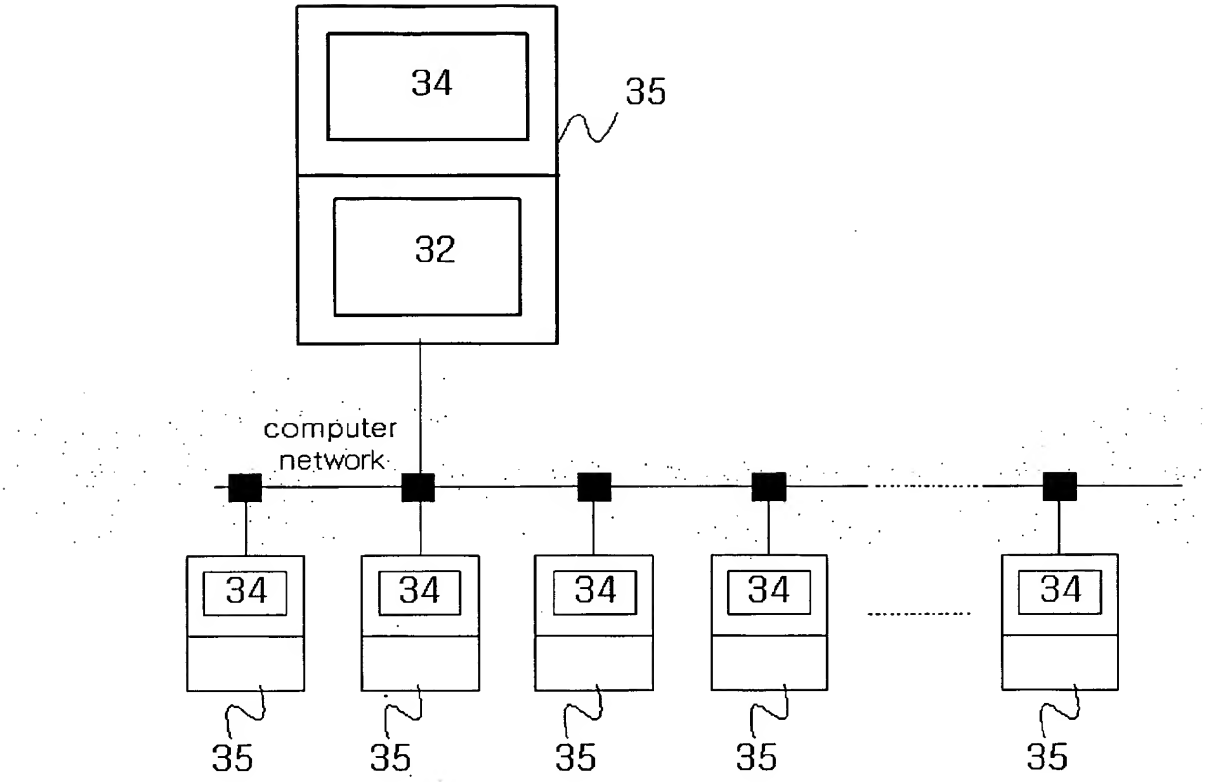
[FIG. 1]

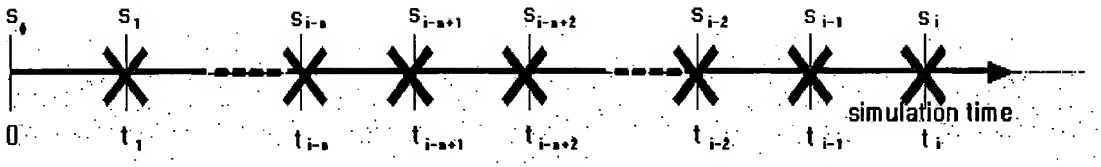


[FIG. 2]



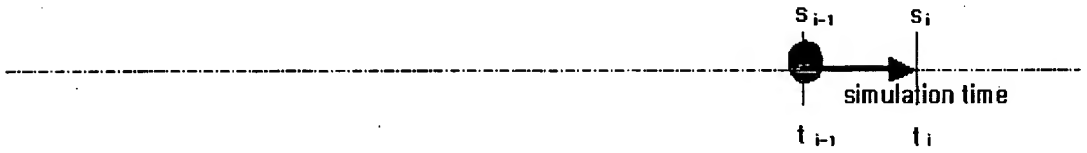
[FIG. 3]

i) 1st simulation



simulation state saving points, or DUV design state saving points, and TB state saving poins, if necessary

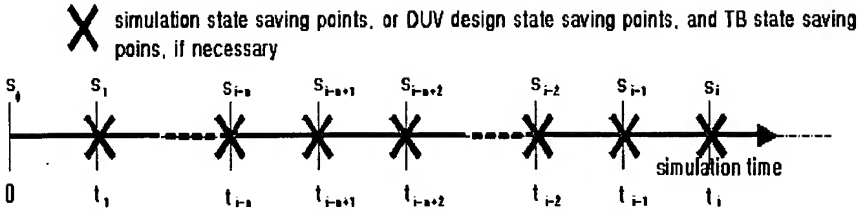
ii) Post-1st simulation



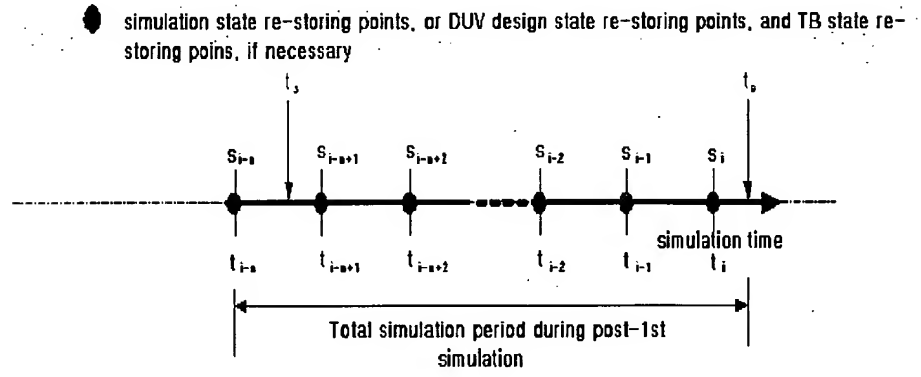
simulation state re-storing points, or DUV design state re-storing points, and TB stat storing poins, if necessary

[FIG. 4]

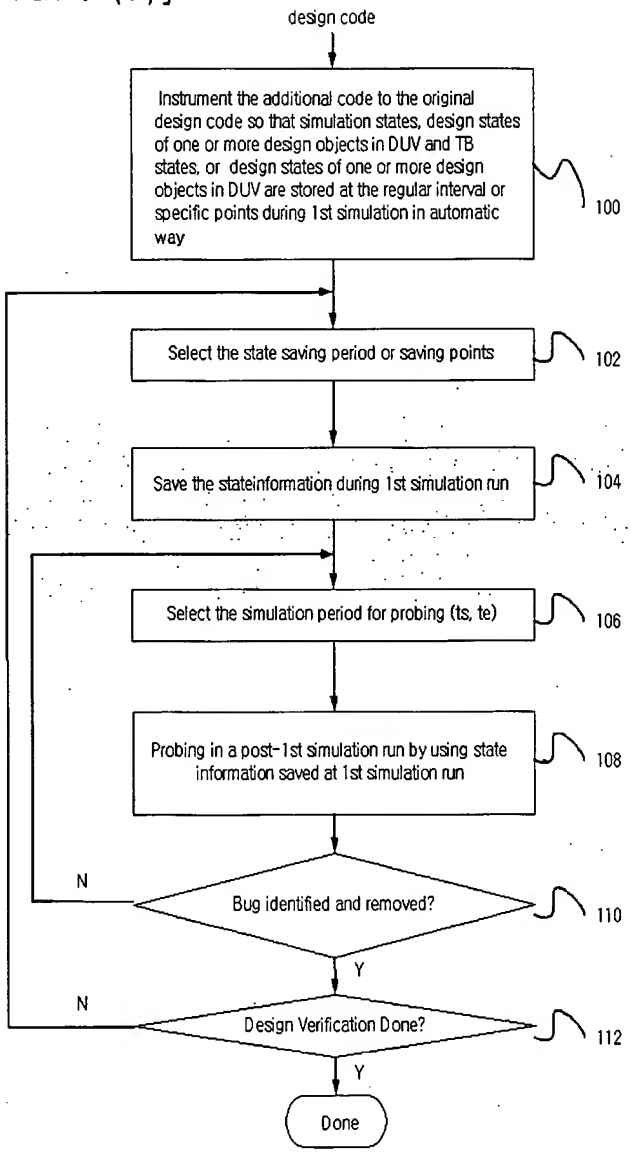
i) 1st simulation



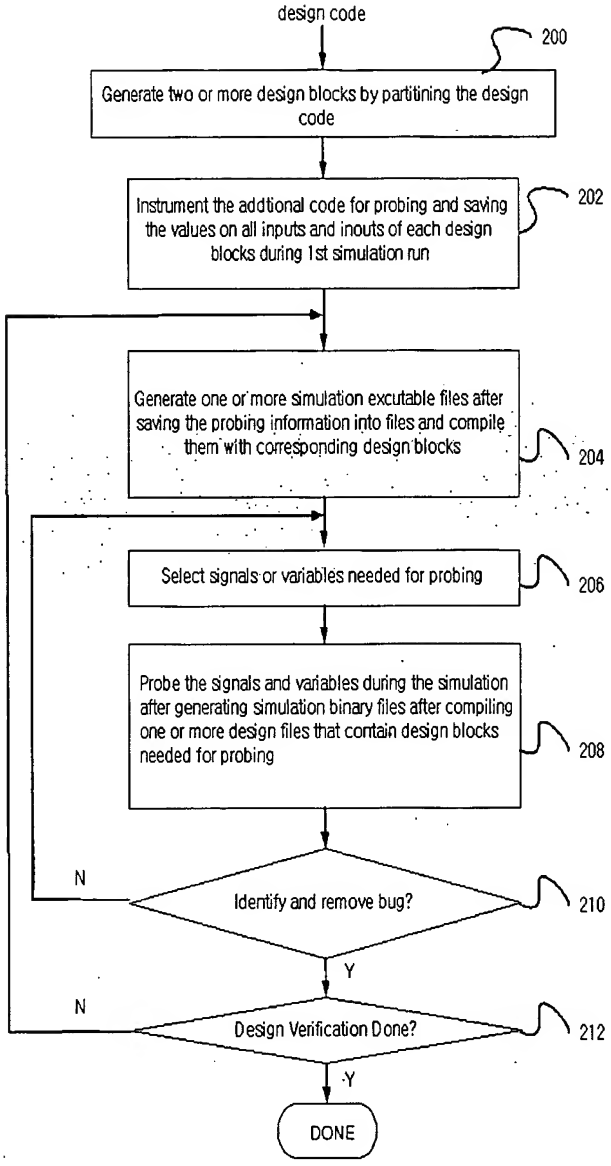
ii) Post-1st simulation



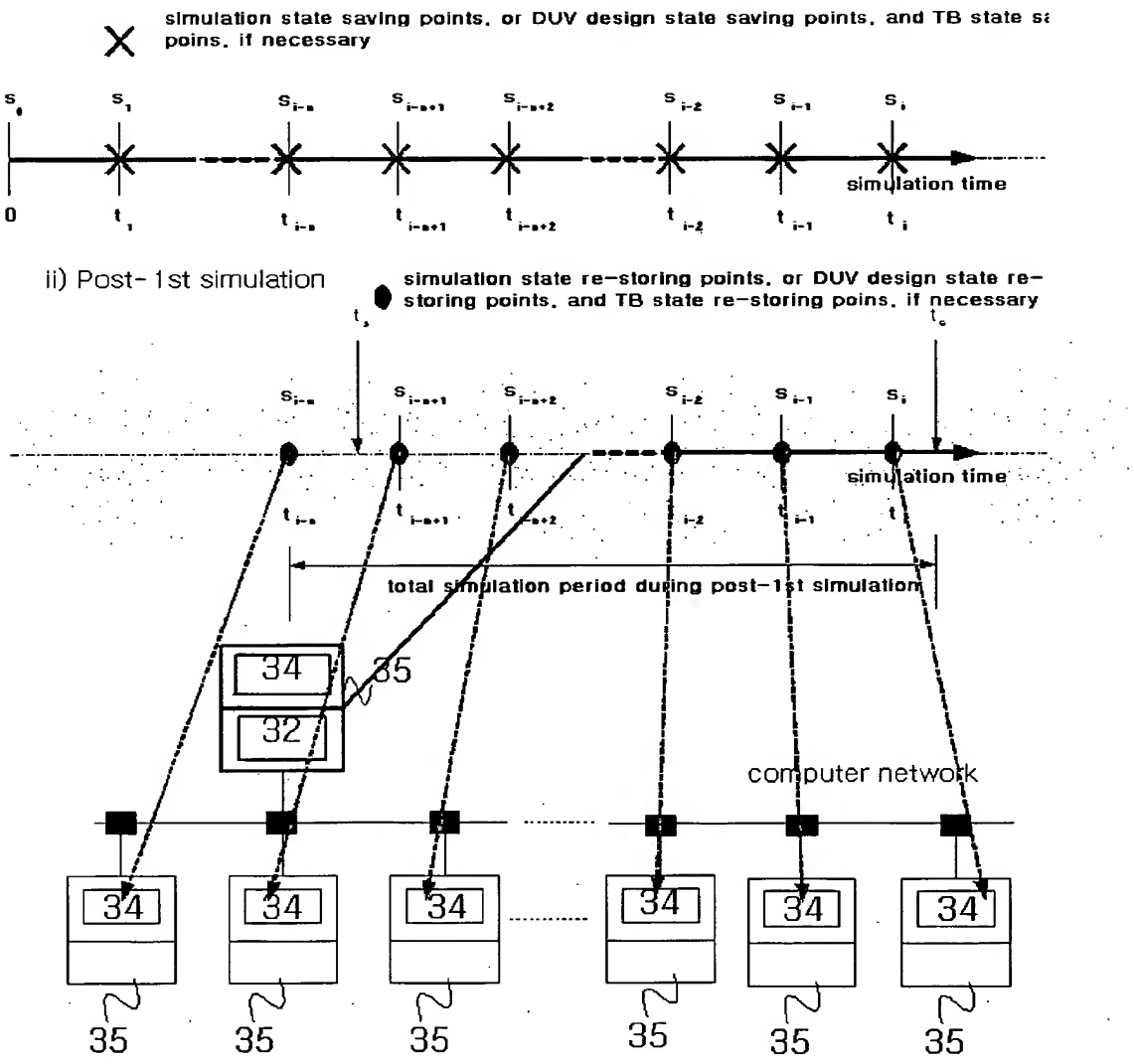
[FIG. 5 (a)]


design code
Instrument the additional code to the original design code so that simulation states, design states of one or more design objects in DUV and TB states, or design states of one or more design objects in DUV are stored at the regular interval or specific points during 1st simulation in automatic way
100
Select the state saving period or saving points
102
Save the stateinformation during 1st simulation run
104
Select the simulation period for probing (ts, te)
106
Probing in a post-1st simulation run by using state information saved at 1st simulation run
108
N
Bug identified and removed?
110
Y
N
Design Verification Done?
112
Y
Done

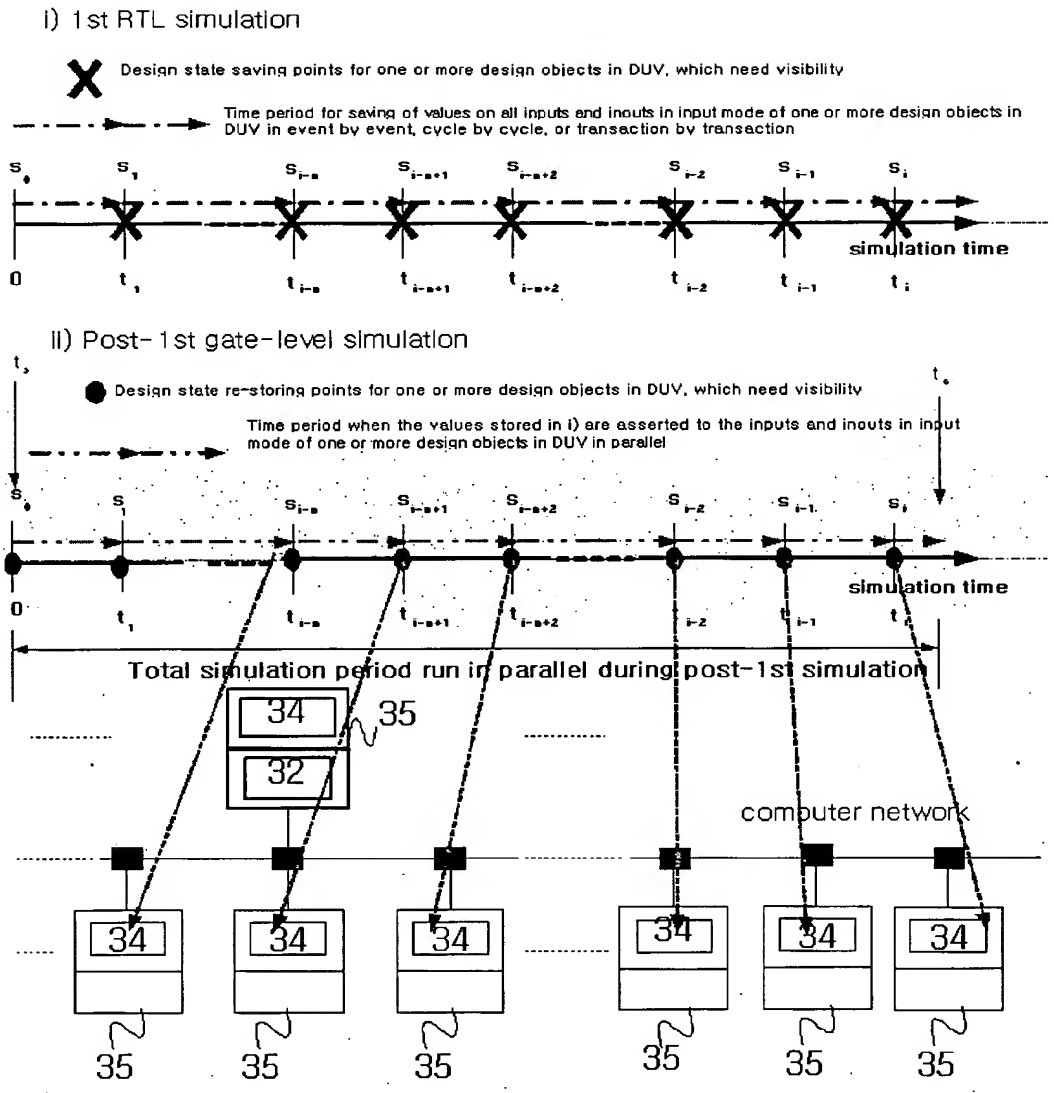
[FIG. 5 (b)]


design code
200
Generate two or more design blocks by partitining the design code
Instrument the addtional code for probing and saving the values on all inputs and inouts of each design blocks during 1st simulation run
202
Generate one or more simulation excutable files after saving the probing information into files and compile them with corresponding design blocks
204
Select signals or variables needed for probing
206
Probe the signals and variables during the simulation after generating simulation binary files after compiling one or more design files that contain design blocks needed for probing
208
N
Identify and remove bug?
210
Y
N
Design Verification Done?
212
Y
DONE

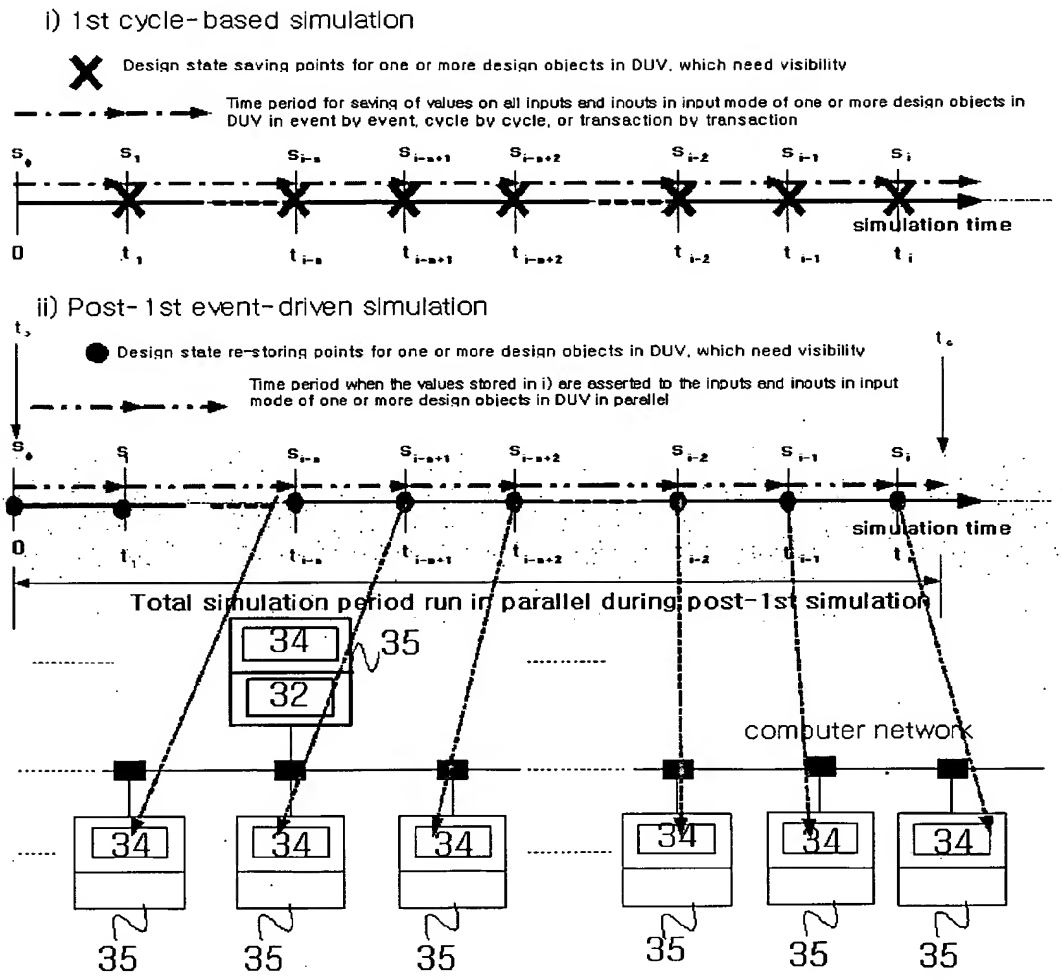
[FIG. 6 (a)]


i) 1st simulation
simulation state saving points, or DUV design state saving points, and TB state sa
poins, if necessary
simulation time
ii) Post-1st simulation
simulation state re-storing points, or DUV design state re-
storing points, and TB state re-storing poins, if necessary
simulation time
total simulation period during post-1st simulation
34
32
35
computer network
34
35

[FIG. 6 (b)]

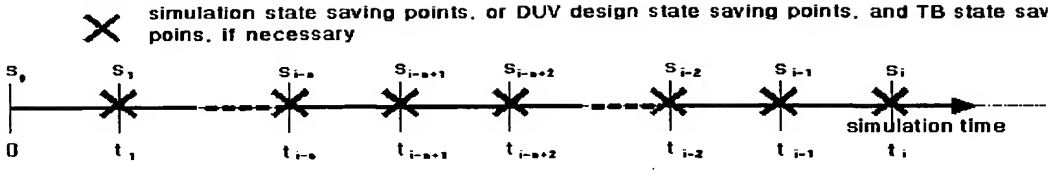

I) 1st RTL simulation
Design state saving points for one or more design objects in DUV, which need visibility
Time period for saving of values on all inputs and inouts in input mode of one or more design objects in DUV in event by event, cycle by cycle, or transaction by transaction
simulation time
II) Post-1st gate-level simulation
Design state re-storing points for one or more design objects in DUV, which need visibility
Time period when the values stored in I) are asserted to the inputs and inouts in input mode of one or more design objects in DUV in parallel
simulation time
Total simulation period run in parallel during post-1st simulation
34
35
32
computer network

[FIG. 6 (c)]

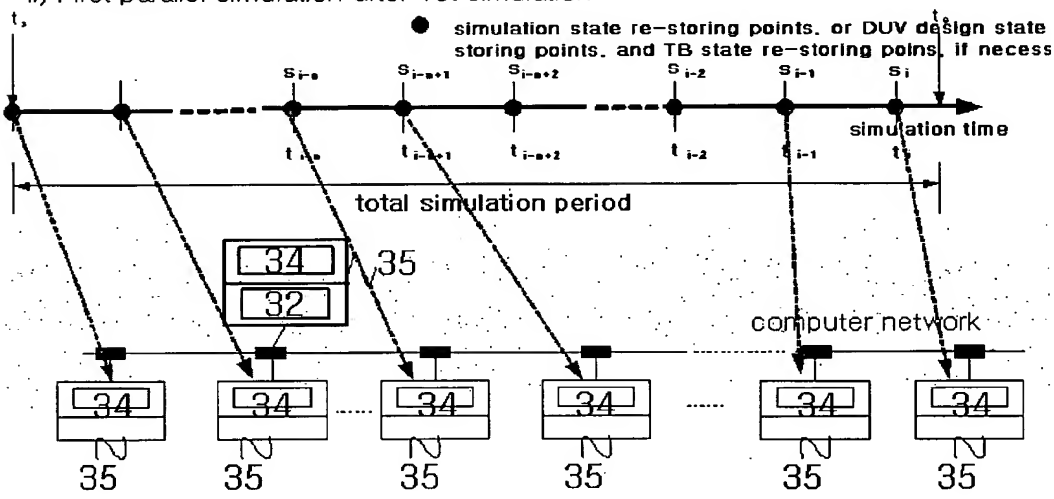

i) 1st cycle-based simulation
Design state saving points for one or more design objects in DUV, which need visibility
Time period for saving of values on all inputs and inouts in input mode of one or more design objects in DUV in event by event, cycle by cycle, or transaction by transaction
simulation time
ii) Post-1st event-driven simulation
Design state re-storing points for one or more design objects in DUV, which need visibility
Time period when the values stored in i) are asserted to the inputs and inouts in input mode of one or more design objects in DUV in parallel
simulation time
Total simulation period run in parallel during post-1st simulation
34
35
32
computer network

[도 6 (d)]

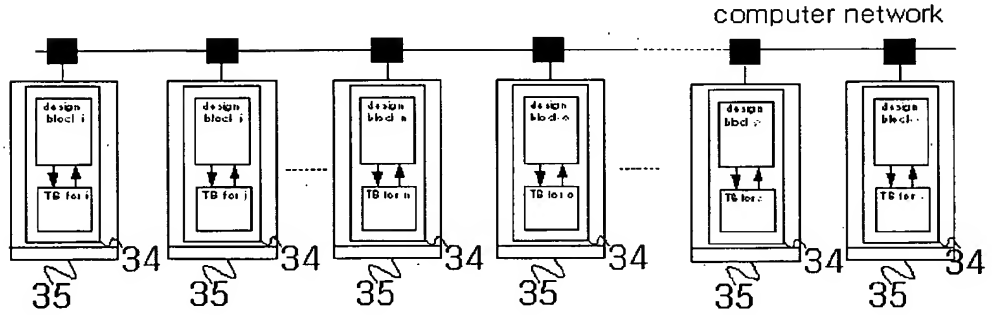
i) 1st simulation



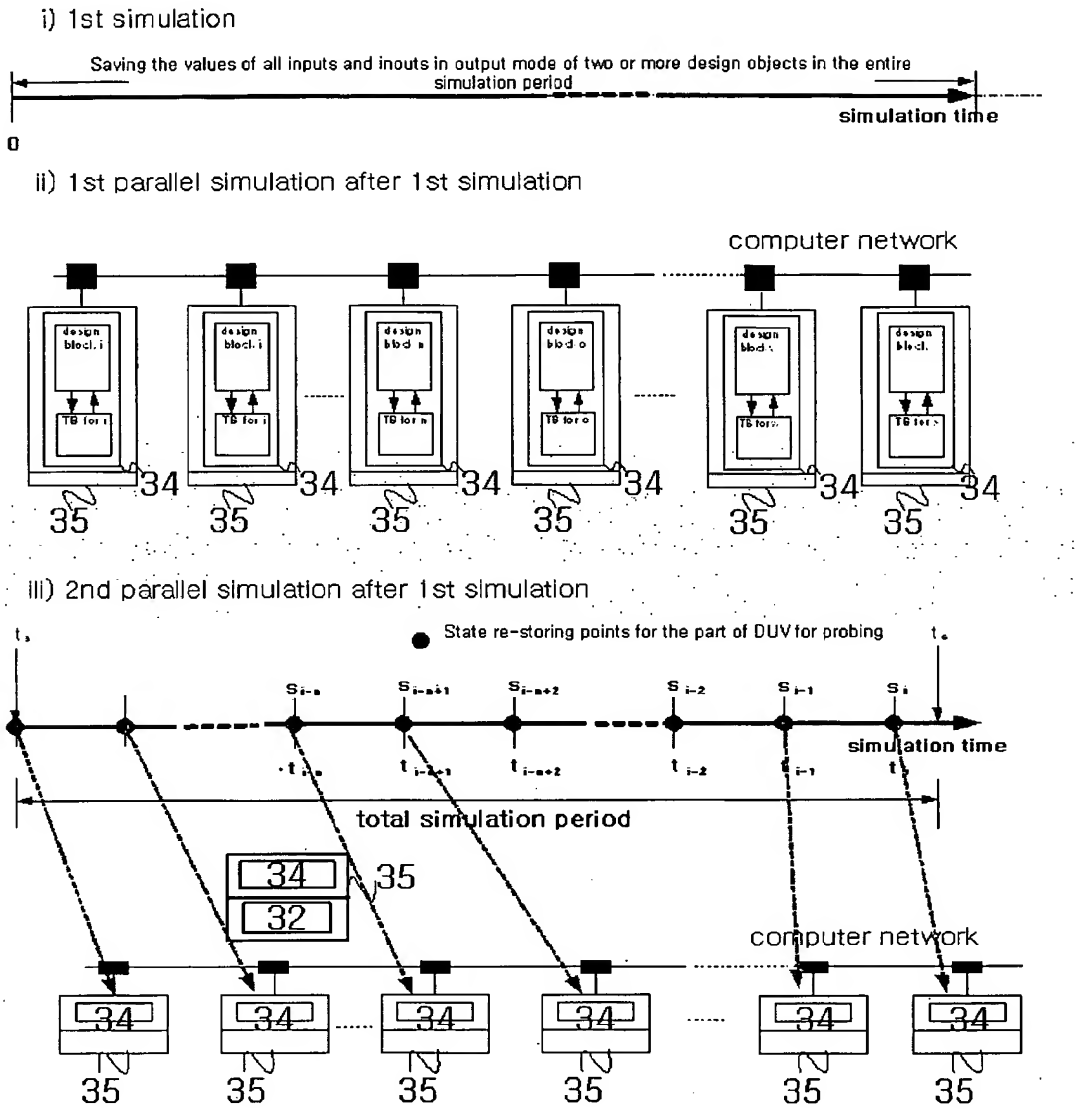
ii) First parallel simulation after 1st simulation



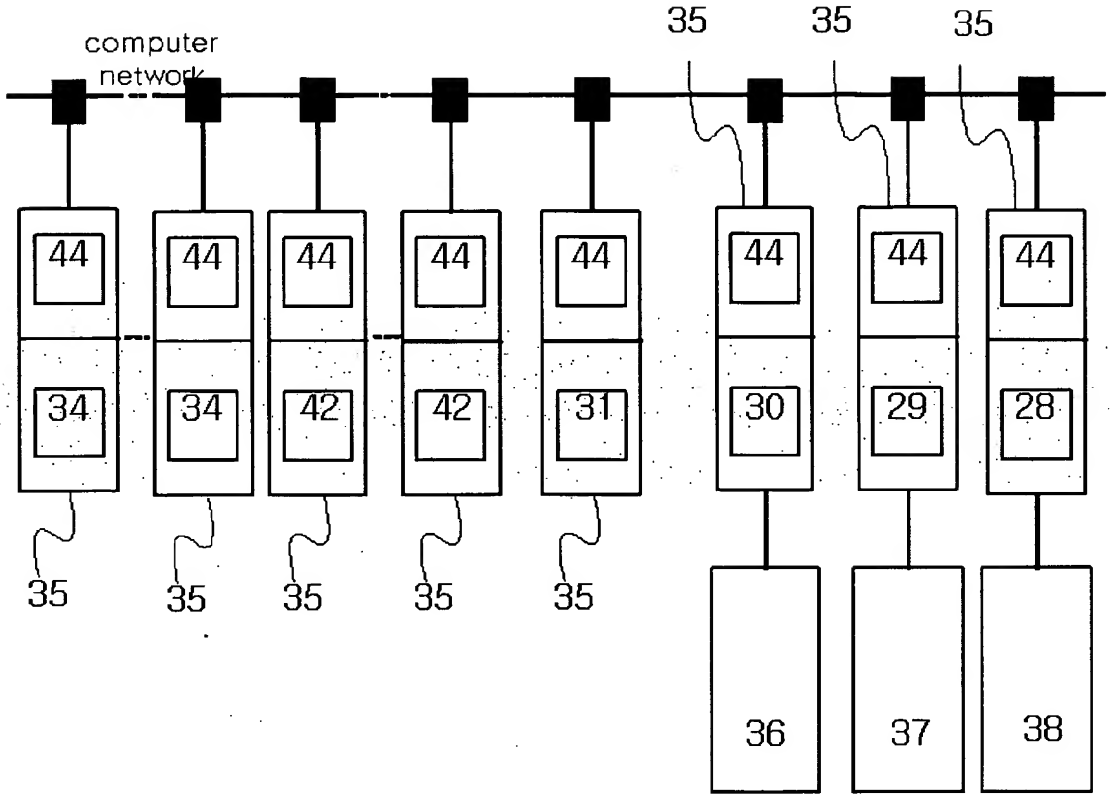
iii) Second parallel simulation after 1st simulation



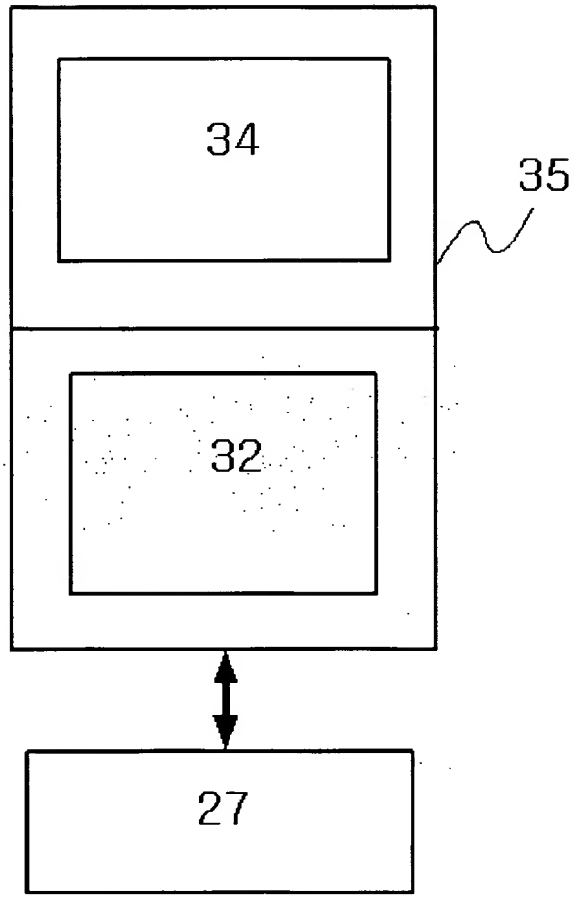
[FIG. 6 (e)]


i) 1st simulation
Saving the values of all inputs and inouts in output mode of two or more design objects in the entire simulation period
simulation time
0
ii) 1st parallel simulation after 1st simulation
computer network
34
35
iii) 2nd parallel simulation after 1st simulation
State re-storing points for the part of DUV for probing
simulation time
total simulation period
34
32
35
computer network

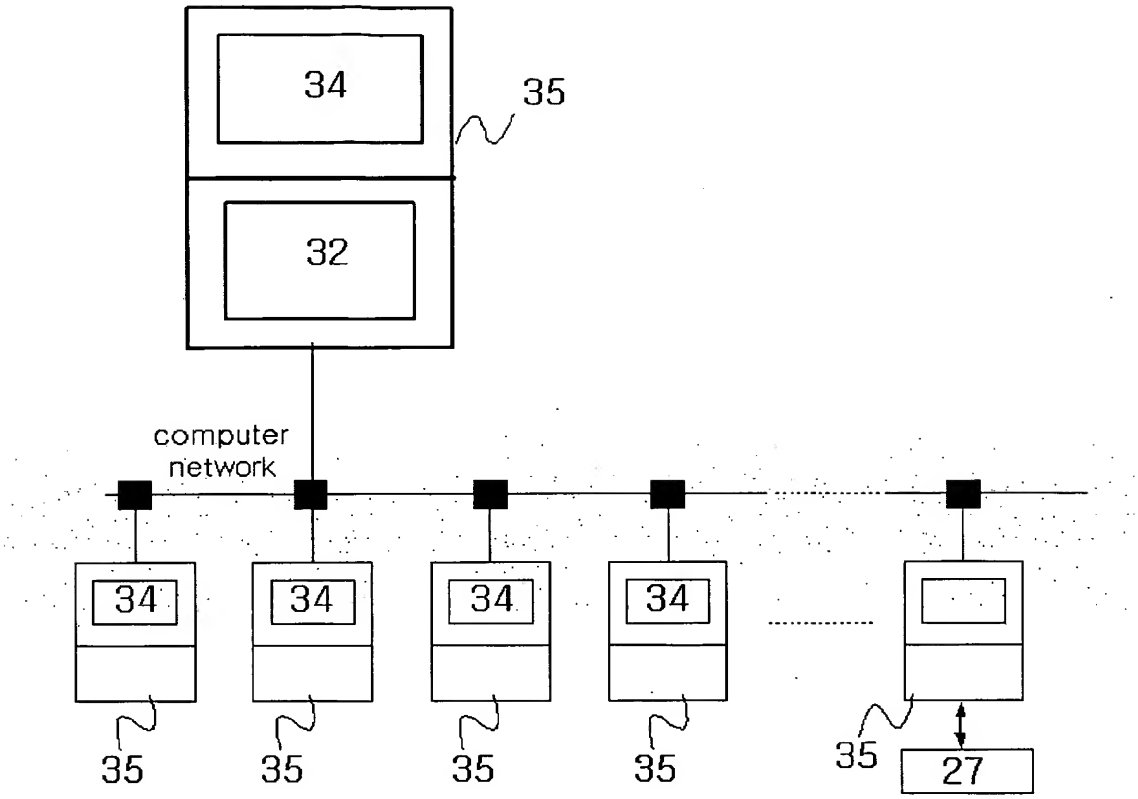
[FIG. 7]



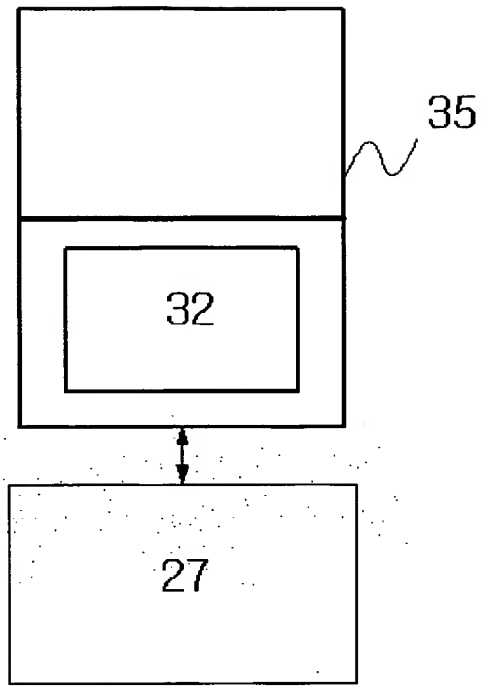
[FIG 8]



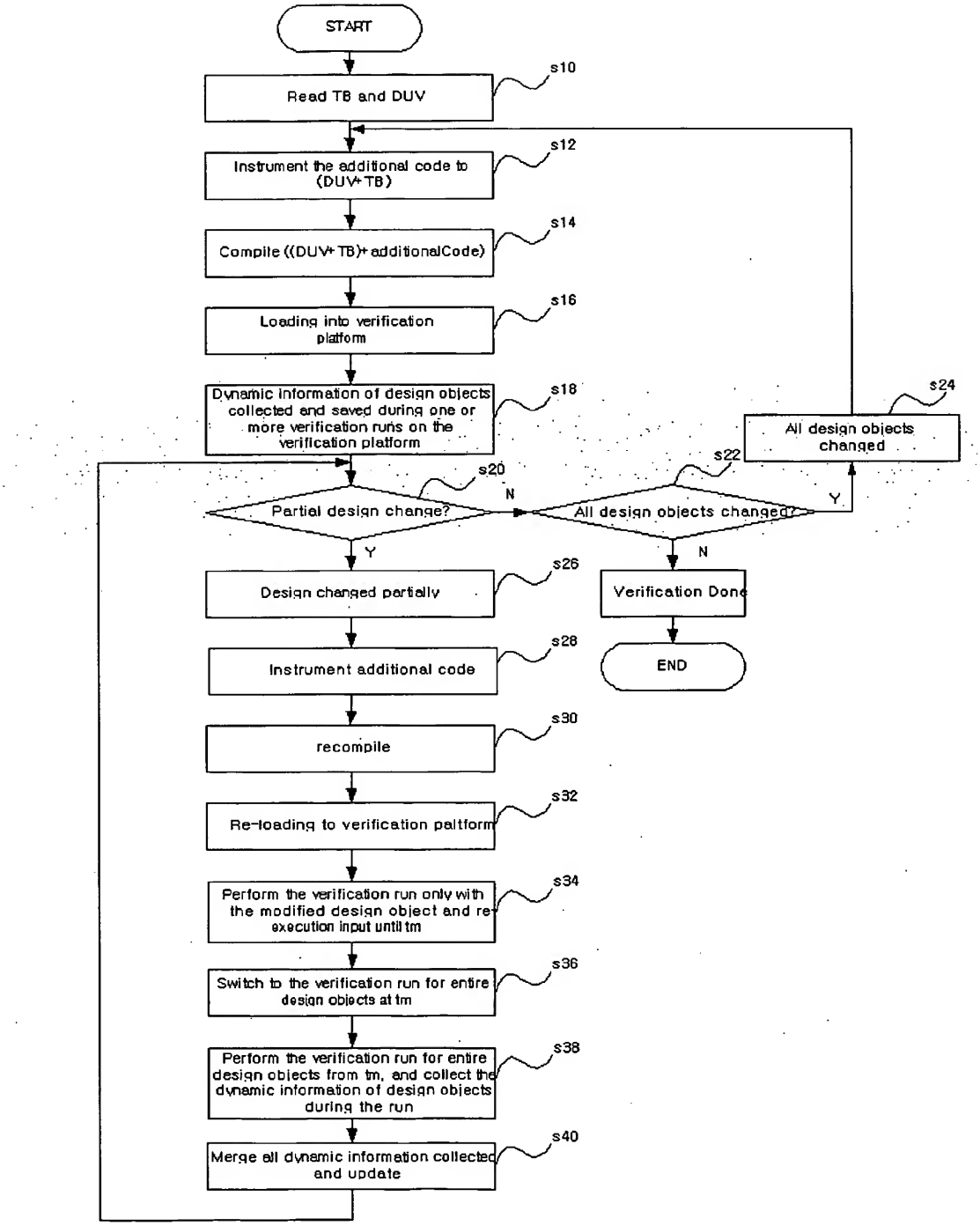
[FIG. 9]



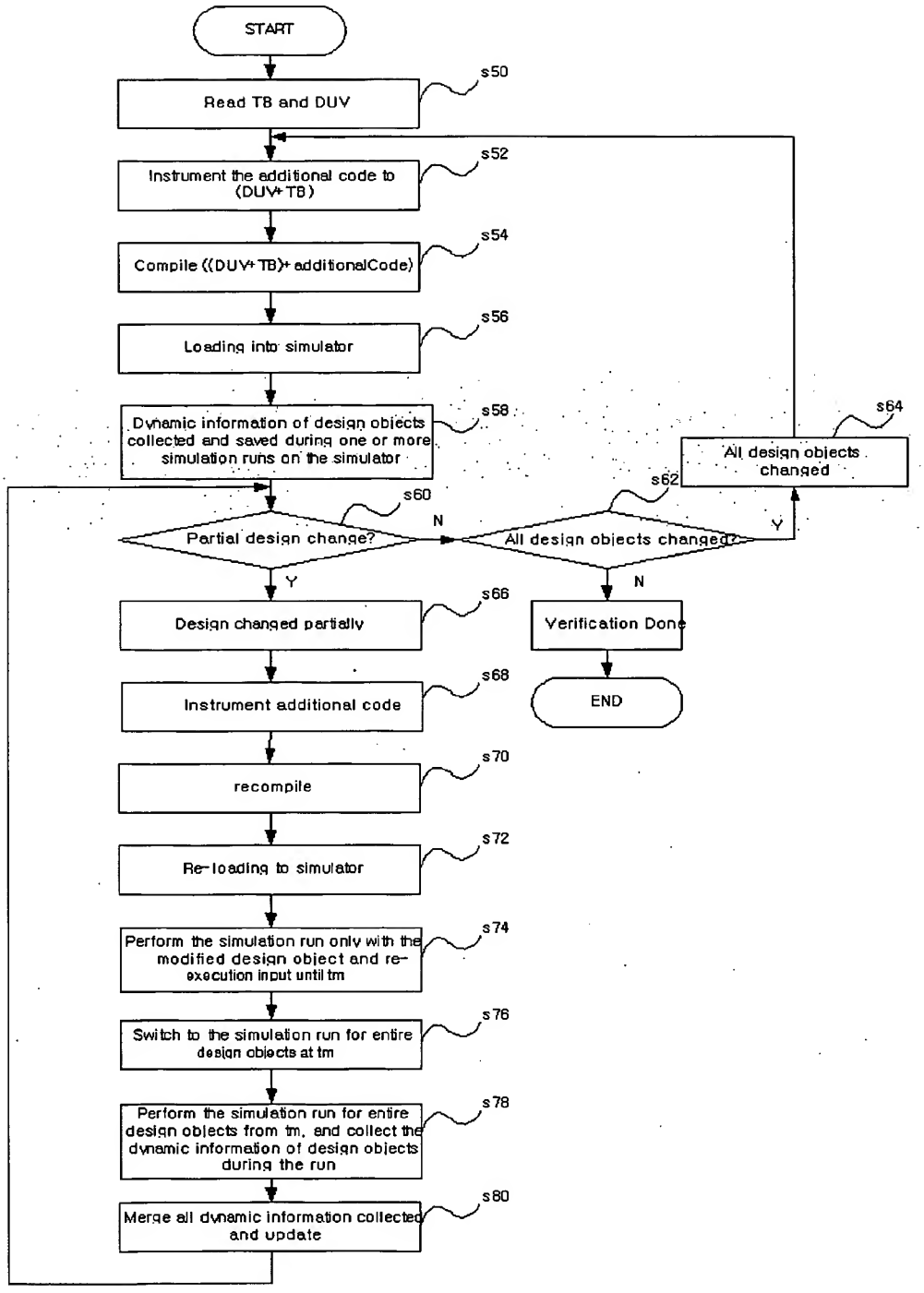
[FIG. 10]



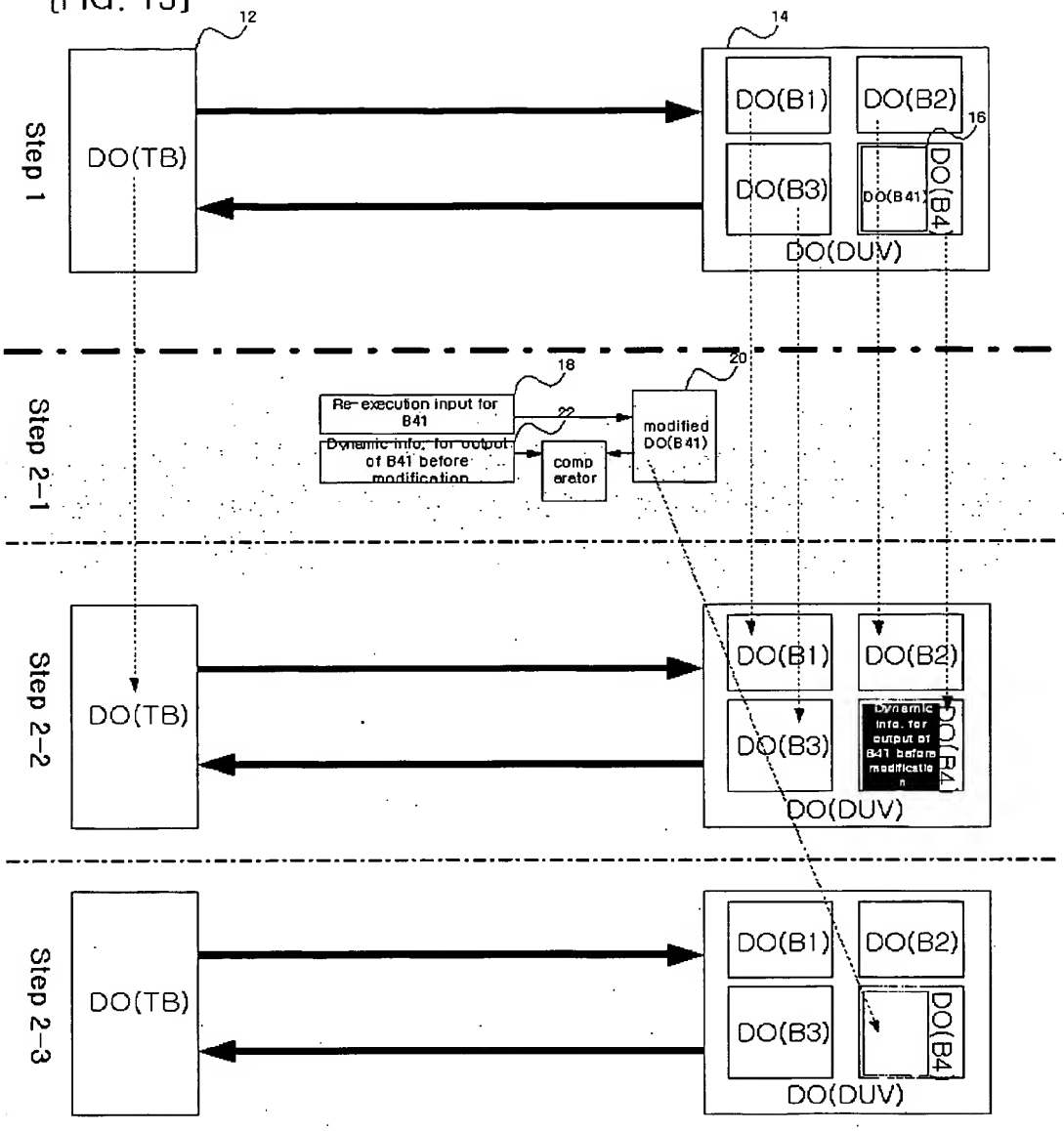
[FIG. 11]


START
s10
Read TB and DUV
s12
Instrument the additional code to (DUV+TB)
s14
Compile ((DUV+TB)+additionalCode)
s16
Loading into verification platform
s18
Dynamic information of design objects collected and saved during one or more verification runs on the verification platform
s20
Partial design change?
N
Y
s22
All design objects changed?
Y
N
s24
All design objects changed
s26
Design changed partially
Verification Done
END
s28
Instrument additional code
s30
recompile
s32
Re-loading to verification paltform
s34
Perform the verification run only with the modified design object and re-execution input until tm
s36
Switch to the verification run for entire design objects at tm
s38
Perform the verification run for entire design objects from tm, and collect the dynamic information of design objects during the run
s40
Merge all dynamic information collected and update

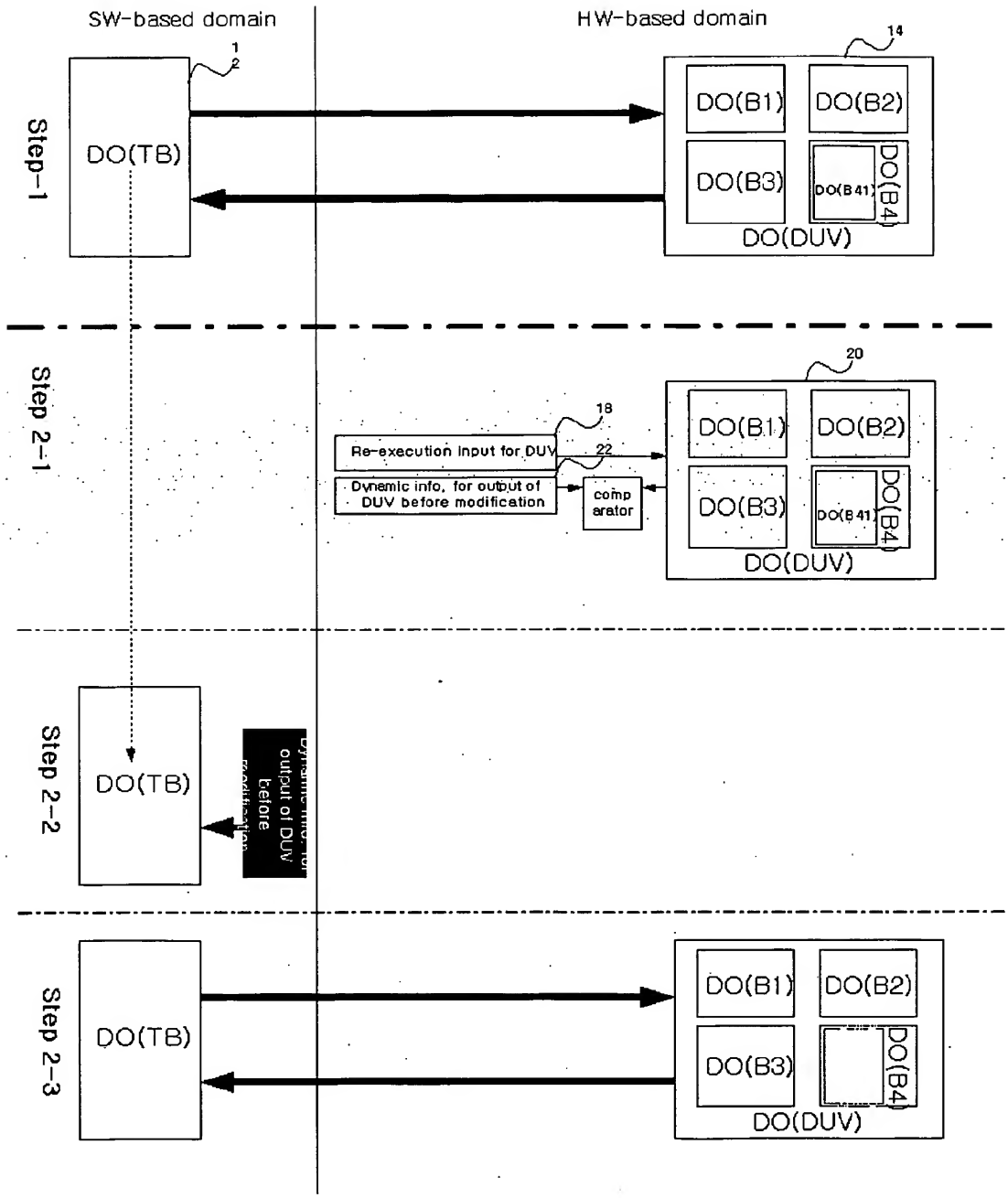
[FIG. 12]


START
Read TB and DUV
s50
Instrument the additional code to (DUV+TB)
s52
Compile ((DUV+TB)+additionalCode)
s54
Loading into simulator
s56
Dynamic information of design objects collected and saved during one or more simulation runs on the simulator
s58
Partial design change?
s60
N
Y
All design objects changed?
s62
Y
N
All design objects changed
s64
Design changed partialy
s66
Instrument additional code
s68
recompile
s70
Re-loading to simulator
s72
Perform the simulation run only with the modified design object and re-execution input until tm
s74
Switch to the simulation run for entire design objects at tm
s76
Perform the simulation run for entire design objects from tm, and collect the dynamic information of design objects during the run
s78
Merge all dynamic information collected and update
s80
Verification Done
END

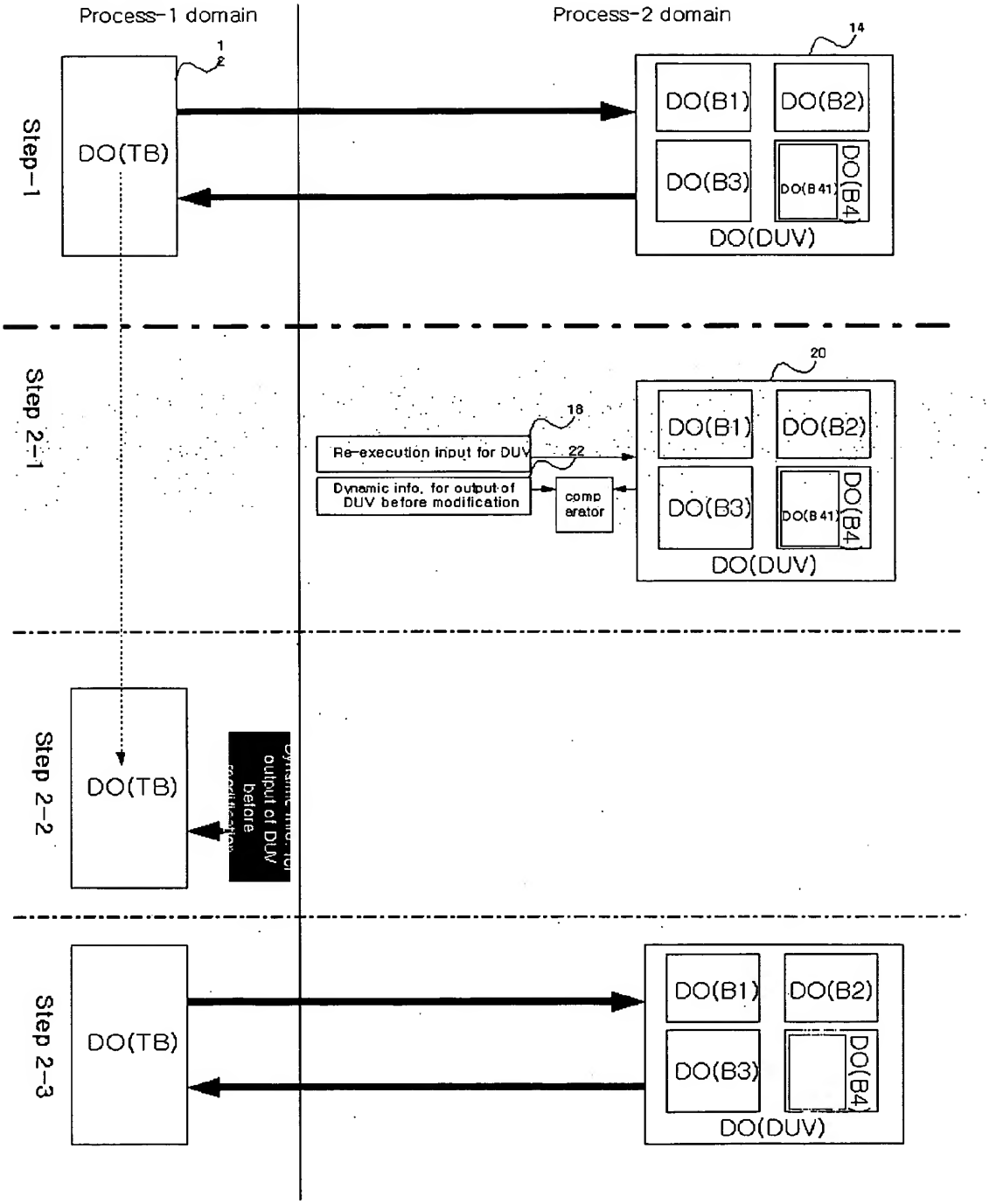
[FIG. 13]


Step 1
DO(TB)
12
14
DO(B1)
DO(B2)
DO(B3)
DO(B4)
DO(B41)
16
DO(DUV)
Step 2-1
18
20
Re-execution input for B41
Dynamic info. for output of B41 before modification
comp aretor
modified DO(B41)
Step 2-2
DO(TB)
DO(B1)
DO(B2)
DO(B3)
Dynamic info. for output of B41 before modificatio n
DO(B4)
DO(DUV)
Step 2-3
DO(TB)
DO(B1)
DO(B2)
DO(B3)
DO(B4)
DO(DUV)

[FIG. 14]


SW-based domain
HW-based domain
Step-1
Step 2-1
Step 2-2
Step 2-3
DO(TB)
DO(B1)
DO(B2)
DO(B3)
DO(B41)
DO(B4)
DO(DUV)
Re-execution input for DUV
Dynamic info. for output of DUV before modification
comp arator
output of DUV before

[FIG. 15]


Process-1 domain
Process-2 domain
Step-1
Step 2-1
Step 2-2
Step 2-3
DO(TB)
DO(B1)
DO(B2)
DO(B3)
DO(B41)
DO(B4)
DO(DUV)
Re-execution input for DUV
Dynamic info. for output of DUV before modification
comp arator
output of DUV before